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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,718	07/22/2003	Soichiro Inaba	FUJI 135	4922

23995 7590 12/15/2005

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1101 14TH STREET, NW  
SUITE 500  
WASHINGTON, DC 20005

EXAMINER

WEINMAN, SEAN M

ART UNIT	PAPER NUMBER
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2115

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/623,718

Applicant(s)

INABA, SOICHIRO

Examiner

Sean Weinman

Art Unit

2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 February 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 7/22/03 8/17/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

### **DETAILED ACTION**

1. Claims 1-12 are presented for examination.

#### ***Drawings***

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "9", "33", and "35" have both been used to designate the "Clock Dividing Ratio Change Setting Circuit". Additionally, reference characters ""29" and "34" have both been used to designate the "Access Wait Changing Circuit". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

#### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US Patent Application Publication 2001/0011356) in view of Flannery (US Patent No. 5,826,092).

As per claim 1, 3, and 4, Lee et al. teach the invention comprising:

a plurality of clock frequencies determined in accordance with a selected one of a plurality of clock change signals (Paragraph [0016] lines 1-6),

a priority order given to the plurality of clock change signals(Paragraph [0013] lines 8-16 and Paragraph [0019] lines 26-36);

a storage unit for storing plural pieces of the system operating condition setting information (Paragraph [0020] lines 1-6) ,

a selector for selecting one of the plurality of clock change signals based on the priority order (Paragraph [0016] lines1-6 and Paragraph [0019] lines 26-36);

and a clock frequency changer (Paragraph [0016] lines1-6);

5. Lee et al. teach a system in which the clock frequency is controlled by a plurality of clock signals. Each clock signal is prioritized to selectively control the clock speed of the system. Additionally, the system has memory that contains setting information for each of the signals as well as a clock control system to select the clock frequency based on priority as well as the setting information. Lee et al. does not explicitly teach that the system is a CPU and that the clock signals control a CPU clock.

6. Flannery teach another system having a computer system that varies the clock speed to conserve power (Col. 3 lines 21-24). Specifically, Flannery teach a power-managed computer which controls the clock speed to conserve power.

7. It would have been obvious to one of ordinary skill in the art to combine Lee et al. and Flannery because they both teach a system in which the clock frequency is controlled in order to conserve power. Furthermore, Flannery covers the deficiency of Lee et al. by teaching the detail that the system in which the clock frequency controlled is a CPU.

8. As per claim 2, Flannery teach the invention comprising:  
a detector for determining whether a memory access is currently performed (Col. 4 lines 50-61)

a plurality of memory access timings corresponding to the plurality of clock change signals (Col. 5 lines 7-12 and Col. 6 lines 40-55 and Figure 2),

and the clock frequency changer is inoperative when the detector determines that the memory access is currently performed (Col. 5 lines 40-46),

and determines the one of the plurality of clock frequencies together with one of the plurality of memory access timings (Col. 5 lines 7-12 and Col. 6 lines 40-55).

As per claim 5, Lee et al. teach the invention comprising:

9. The priority order is decided in accordance with a value of a clock frequency determined with each of the clock change signals (Paragraph [0013] lines 8-16 and Paragraph [0019] lines 26-36).

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US Patent Application Publication 2001/0011356) and Flannery (US Patent No. 5,826,092) as applied to claims 1-5 above, and further in view of Iwazaki (US Patent No. 6,073,244).

11. Lee et al. and Flannery teach a CPU in which the clock frequency is controlled by a plurality of clock signals. Each clock signal is prioritized to selectively control the clock speed of the system. Additionally, the system has memory that contains condition setting information for each of the signals as well as a clock control system to select the clock frequency based on priority as well as the condition setting information. However, Lee et al. and Flannery fail to detail the invention where there is a clock stop unit and a clock cancellation unit in response to the clock change signals.

12. Iwazaki teaches a power savings clock control apparatus having a clock stop control unit, additionally, a clock restart control circuit in order to control the clock frequency to conserve power.

a clock stop unit for preventing the passage of a clock signals and a stop cancellation unit to resume passage of a clock signal in response to a clock change signal (Col. 7 lines 45-62).

13. It would have been obvious to one of ordinary skill in the art to combine the teachings of Lee et al. and Flannery along with Iwazaki because they teach a power saving clock control apparatus for a system. Iwazaki covers the deficiency of Lee et al. and Flannery by teaching the detail of the clock control apparatus having a stop clock and stop clock cancellation unit.

14. As per claims 7-12, it is directed to the means of the clock control apparatus as set forth in claims 1-6. Since Lee et al. and Flannery along with Iwazaki teach the claimed clock control apparatus; Lee et al. and Flannery along with Iwazaki teach the means for the claimed clock control apparatus.

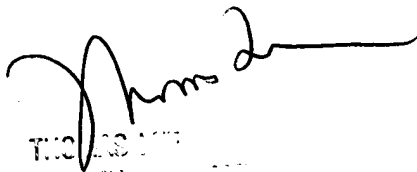
**Conclusion**

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean Weinman whose phone number is (571) 272-2744. The examiner can normally be reached on Monday-Friday from 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sean Weinman  
Examiner  
Art Unit 2115



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